REMARKS

The foregoing amendment is provided to prepare the present application for issuance. No new matter has been added.

Claims 15-18, 24-33 and 35-38 are allowed. Claims 36 and 38 are cancelled.

Applicants respectfully requests the Examiner enter the above amendments. If the Examiner believes a telephone conference would expedite or assist, the Examiner is invited to call John Ward at (408) 720-8300, x237.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

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Date:10/30/2002

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The paragraph beginning on page 4, line 3, has been amended as follows:

Figure 9 illustrates one embodiment of a method followed by a processor when performing an unpack operation on packed data.

The paragraph beginning on page 9, line 11, has been amended as follows:

Depending on the type of data, the data may be stored in integer registers 201, registers 209, status registers 208, or instruction pointer register 211. Other registers can be included in the register file 204, for example, floating point registers. In one embodiment, integer registers 201 store thirty-two bit integer data. In one embodiment, registers 209 contains eight registers, R_0 212a through R_7 212h. Each register in registers 209 is sixty-four bits in length. R_0 212a, R_1 212b and R_2 212c are examples of individual registers in registers 209. Thirty-two bits of a register in registers 209 can be moved into an integer register in integer registers 201. Similarly, a[n] value in an integer register can be moved into thirty-two bits of a register in registers 209.

The paragraph beginning on page 16, line 1, has been amended as follows:

Figure 5b through Figure 5d illustrate the in-register packed data storage representation. Unsigned packed byte in-register representation 510 illustrates the storage of packed byte 501 in one of the registers R_0 212a through R[n]7 212[af]h. Information for each byte data element is stored in bit seven through bit zero for byte zero, bit fifteen through bit eight for byte one, bit twenty-three

through bit sixteen for byte two, bit thirty-one through bit twenty-four for byte three, bit thirty-nine through bit thirty-two for byte four, bit forty-seven through bit forty for byte five, bit fifty-five through bit forty-eight for byte six and bit sixty-three through bit fifty-six for byte seven. Thus, all available bits are used in the register. This storage arrangement increases the storage efficiency of the processor. As well, with eight data elements accessed, one operation can now be performed on eight data elements simultaneously. Signed packed byte in-register representation 511 is similarly stored in a register in registers 209. Note that only the eighth bit of every byte data element is the necessary sign bit; other bits may or may not be used to indicate sign.

Table 1, on page 20, has been amended as follows:

Data Format	Minimum Value	Maximum Value
Unsigned Byte	0	255
Signed Byte	-128	127
Unsigned Word	0	65535
Signed Word	-32768	32767
Unsigned Doubleword	0	$2^{[64]32}-1$
Signed Doubleword	$-2^{[63]31}$	$2^{[63]31}-1$

Table 1

IN THE CLAIMS:

Claims 36 and 38 are cancelled.